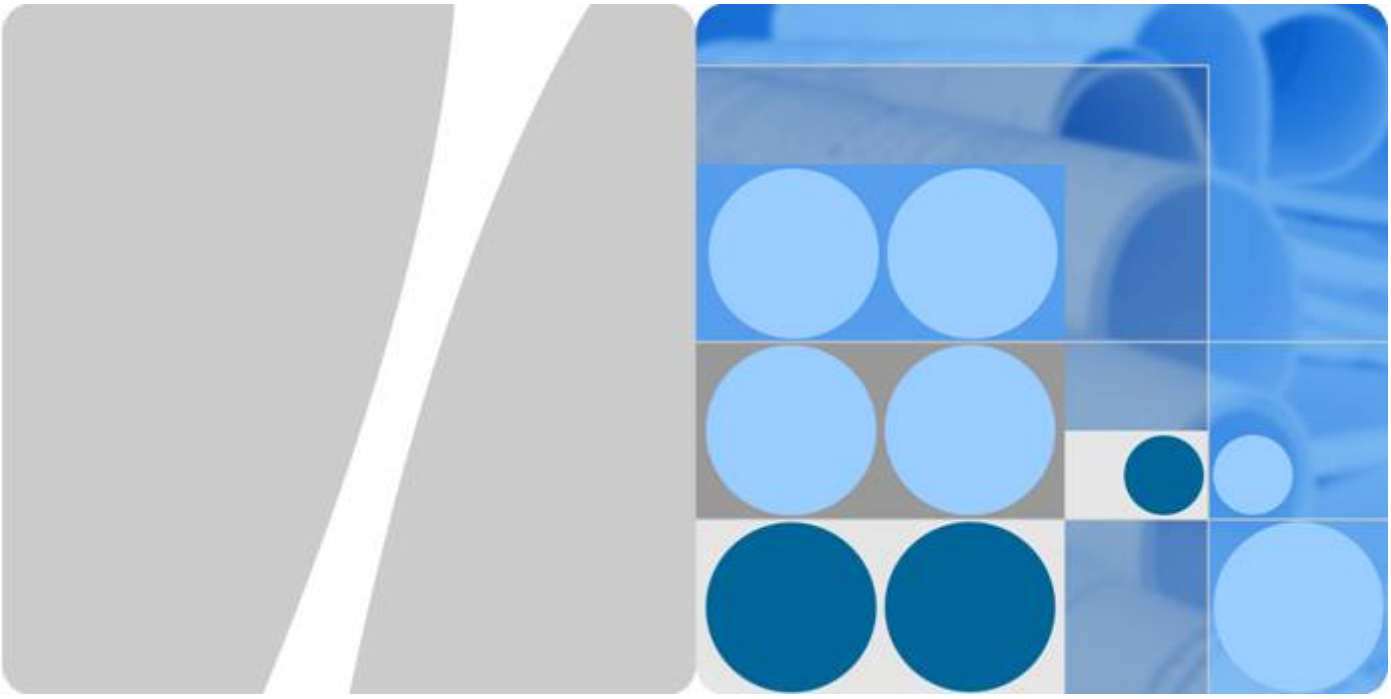


FPGA-accelerated Cloud Server

User Guide

Date **2019-03-30**

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1 Overview

Introduction

FPGA-accelerated Cloud Server (FACS) provides tools and environments for you to develop and use Field Programmable Gate Arrays (FPGAs). With FACSs, you can easily develop FPGA accelerators and deploy easy-to-use, cost-effective, agile, and secure FPGA-based services.

The following types of FACSs are available:

- FACSs using a high-performance architecture

  FACSs of this type are based on a high-performance DPDK interaction framework and support the flow calculation model and data flow concurrency. They are designed for RTL development and meet the requirements of high bandwidth and low latency.
- FACSs using a universal architecture

  FACSs of this type are based on a general-purpose SDAccel interaction framework and support the block calculation module and Xilinx Scatter-Gather DMA (SGDMA) data transmission. They are designed for advanced language development or existing algorithm transplantation and meet the requirements of fast service rollout.

Application Scenarios

FACS provides a Hardware Develop Kit (HDK) and Software Develop Kit (SDK) to develop and apply Accelerated Engine Images (AEIs).

FACS provides FPGAs with high computing performance, which can be used for applications that require high-performance parallel computing, such as machine learning, search engine, and artificial intelligence (AI).

Basic Concepts

- HDK: contains accelerator examples, coding environment, simulation platform, automatic compilation tools, and code encrypting and debugging tool packages.
- SDK: contains application examples, hardware abstract interfaces, accelerator abstract interfaces, accelerator drivers and runtime, and the version management tool.

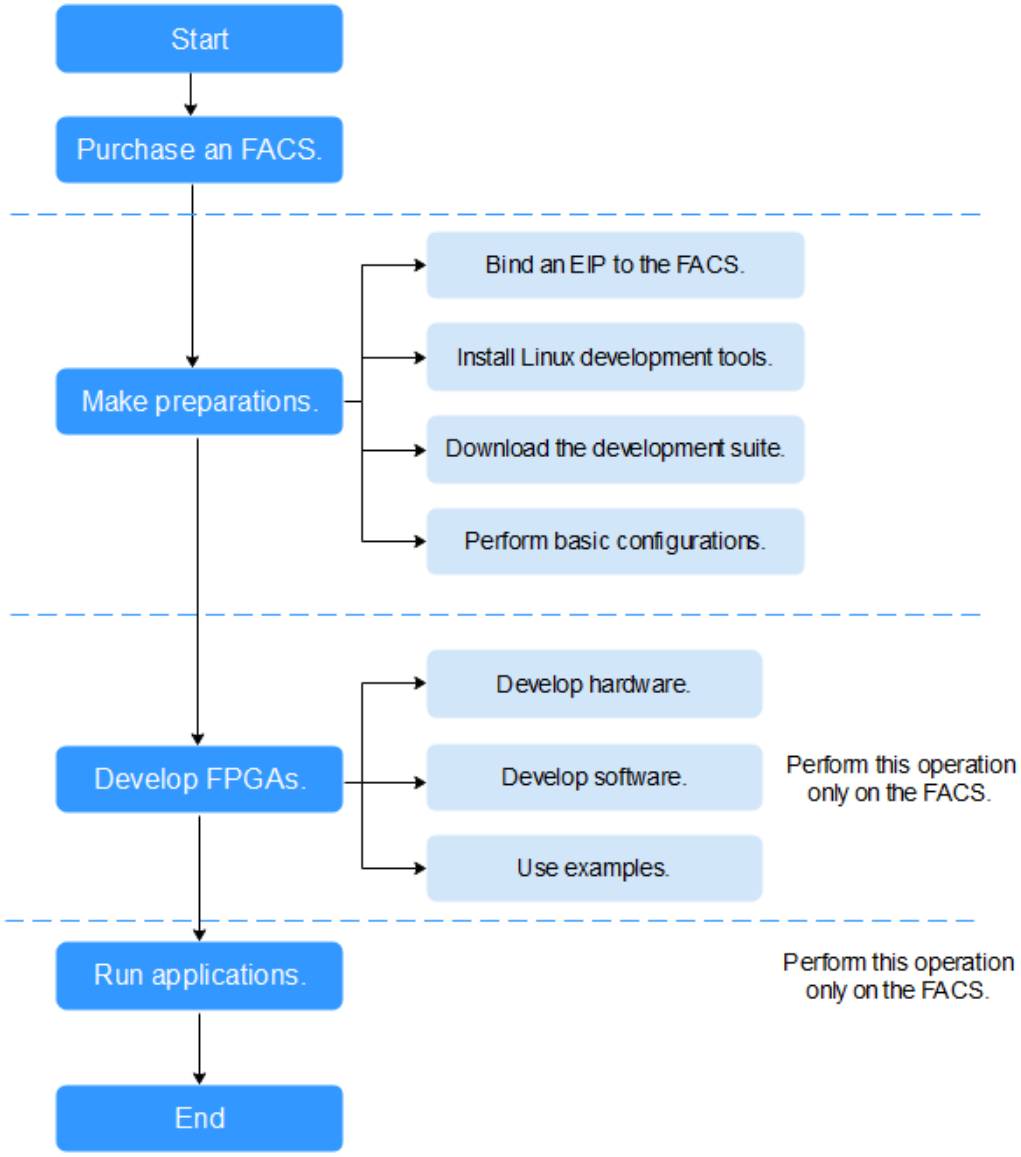
- AEI: an acceleration instance developed by users on Open Telekom Cloud
- FPGA: a gate-level programmable component which implements complex combination or timing logic by using a Verilog- or VHDL-based circuit design.
- Image: Elastic Cloud Server (ECS) image

Process

FACS provides the GitHub open-source web service platform, allowing you to integrate FACSs to a third-party system for secondary development.

Figure 1-1 shows the process of using FACS.

Figure 1-1 Process of using FACS



2 Purchasing an FACS

Purpose

Before you can start developing FPGAs, log in at **HUAWEI CLOUD** and purchase an FACS. For details, see **Methods of Purchasing ECSs**.

NOTE

When using the FACS, you need to install some development tools, which occupy a large amount of disk space. Therefore, when purchasing an FACS, ensure that the system disk size is greater than or equal to 100 GB. You are advised to select a 100 GB system disk.

Application Scenarios

Use the FACS service for the first time or repurchase an FACS.

Login Method

Use an SSH password to log in to a Linux FACS. For details, see **Login Using an SSH Password**.

3 Preparations

3.1 Binding an EIP to an FACS

When using an FACS, you need to download development tools using an elastic IP (EIP) address. For details about how to bind an EIP to an FACS, see **Assigning an EIP and Binding It to an ECS**.

NOTE

If you have bound an EIP to your FACS during creation, skip this section.

3.2 Downloading the Development Suite

After purchasing an FACS, obtain or update the FPGA development suite from the GitHub platform. For details about how to obtain the suite, see "Downloading Suite" in **README**.

3.3 Installing and Configuring fisclient

To manage AEIs, you need to install and configure fisclient based on **README**.

For how to install fisclient, see **Installing fisclient**.

For how to configure fisclient, see **Configuring fisclient**.

4 Developing FPGAs and Running Applications

FACS provides an HDK and an SDK.

The HDK contains accelerator examples, coding environment, simulation platform, automatic compilation tools, and code encrypting and debugging tool packages. You can quickly develop and test your FPGA hardware accelerator by referring to the application examples and development guide.

The SDK contains application examples, hardware abstract interfaces, accelerator abstract interfaces, accelerator drivers and runtime, and the version management tool. Accelerator abstract interfaces allow your applications to invoke the hardware accelerator in the same way as the software function library, helping you easily develop high-performance applications based on the hardware accelerator.

How Direct Connect works

Use the suite to develop FPGAs.

Developing FPGAs and Running Applications

For details about how to develop hardware and applications using the FP1 development suite, see **README**.

NOTE

To obtain the historical FP1 versions, see **release_note.md** and download the corresponding tag.

Table 4-1 Historical FP1 versions

No.	Tag	High-Performance Architecture Shell ID	Universal Architecture Shell ID
1	V1.0.0	01010023	01210002
2	V1.0.1	01010023	01210002

No.	Tag	High-Performance Architecture Shell ID	Universal Architecture Shell ID
3	V1.1.0	01010028	01210005
4	V1.1.1	01010028	01210005
5	V1.1.2	01010028	01210006
6	V1.2.0	01010029	01210101
7	V1.2.1	01010029	01210101
8	V1.3.0	0101002e	01210106

NOTE

For how to obtain the Shell ID, see section "Querying the Status of an FPGA Card Image" in **FpgaCmdEntry Operation Instructions**.

A Change History

Release On	Description
2019-03-30	This issue is the eleventh official release. Added the historical FP1 versions in **4 Developing FPGAs and Running Applications**.
2018-12-24	This issue is the tenth official release. Deleted the content for Open Beta Test.
2018-11-27	This issue is the ninth official release. Updated the path for downloading the historical version of the development suite in **3.2 Downloading the Development Suite**.
2018-10-22	This issue is the eighth official release. Updated the README links in **3.2 Downloading the Development Suite**.
2018-09-25	This issue is the seventh official release. Updated **3.2 Downloading the Development Suite**.
2018-06-30	This issue is the sixth official release. • Updated the development suite version in **3.2 Downloading the Development Suite**. • Deleted section "Configuring the Internal DNS".
2018-04-30	This issue is the fifth official release. • Added section "Configuring the Internal DNS". • Optimized **3.3 Installing and Configuring fisclient**. • Added section **Binding an EIP to an FACS**.
2018-01-25	This issue is the fourth official release. • Added section "A.1.4 Association Subcommand". • Added section "A.1.5 Disassociation Subcommand". • Added section "A.1.6 Query Subcommand".

Release On	Description
2017-10-27	This issue is the third official release. Added information about how to develop and apply AEIs based on the FPGA development and simulation suites of the Vivado and SDAccel tools.
2017-10-10	This issue is the second official release. ● Added "Appendix A.4 Known Issues of the SDK". ● Updated command descriptions.
2017-08-10	This issue is the first official release.